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A Bubble Memory Differential Detector

By W. D. WYNN

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In the application of digital memories, significant variations can occur in the memory sensor analog responses processed by detection circuitry to recover stored binary data. Across an ensemble of memory devices of the same type, the variations are due to manufacturing deviations, and for a particular device, they occur with changes in operating conditions. With magnetic bubble memories, binary data are recovered by sensing the presence or absence of a magnetic domain in each bit interval. In general, a nonadaptive bubble detector does not accommodate the variations that may occur in the bubble response when each decision is based only on the sensor response in the current bit interval. Here we present a differential detector design that is reasonably simple to implement as one integrated circuit and is tolerant of signal amplitude drifts in bubble memory sensor outputs.

I. INTRODUCTION

In typical field-accessed magnetic bubble memories (MBM), stored binary data on memory chips are detected by processing millivolt-level signals that are measured differentially across a matched pair of permalloy magnetoresistive sensor strips.[1-3] Ideally these sensors are subjected to the same magnetic, electrical, and environmental conditions with the exception that only one, the active sensor, is subjected to H fields of traversing bubble domains. In the drive field period of a field-accessed MBM chip, by design at least one time interval exists, defined here as the detection interval (DI), in which the sensor differential response is relatively free of unavoidable signal interferences such as MBM function drive crosstalk and sensor magnetoresistive switching noise. Within the DI a detectable difference should exist between responses for the bubble and no-bubble cycles of the memory. Even after carefully choosing the DI, undesirable sensor response variations can still occur. Variations within the DI that have been of major concern in the use of previous nonadaptive MBM detectors are

the device processing variation in magnetoresistive sensor response, the negative temperature coefficient of this response, the phase shift of bubble response transition tbat occurs with chip manufacturing and drive field changes, and the adjacent symbol interaction of bubbles in the sensor array. In a detector where the DI is fixed and where the individual bubble response in the DI is compared to a fixed threshold these variations have been intolerable.

An accurate analytical parametric description of the family of sensor signals that are observed for any MBM chip type has been intractable because of the nonlinear field effects of permalloy magnetoresistive sensor arrays and a lack of models for statistical data about the manufacturing variations for MBM devices. Figure 1 shows qualitative examples of differenced sensor responses within a DI that may exist for a chip type when the manufacturing and operational variations are considered. Each signal pair is shown in the DI for some particular chip of an ensemble of the same chip type at a particular operating condition. All signals have been referenced to a voltage V_r at the start of the DI. The amplitude and time scales for Fig. 1 are representative of field-accessed MBMs with field drive frequencies in the 100-kHz range. Not only can response amplitude change with operating conditions and selected chip, but also the shape of the desired bubble response and intersymbol interference contributions may vary.

Detectors could be designed that adapt to variations in the bubble and no-bubble responses where such variations preclude a fixed threshold detector. For example, detector amplifier gains could be temperature compensated to track the temperature sensitivity of the magnetoresistive sensor. Also, the phase of the DI could be adaptive, and detection thresholds could be adjusted dynamically from responses in a known data pattern. Unfortunately, adaptive bubble detectors have disadvantages such as increased circuit complexity, increased cost, and system limitations such as detector adaptation time before reading data.

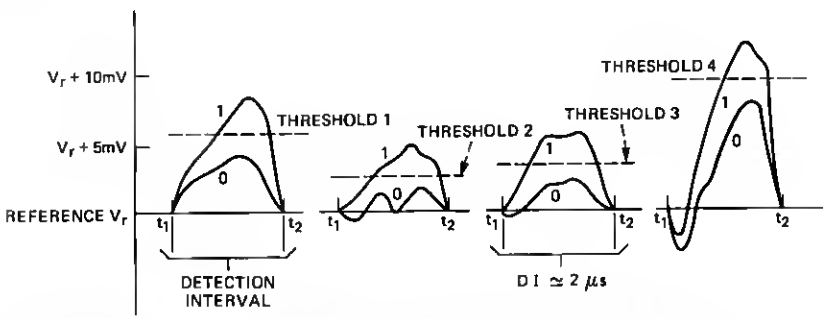

Fig. 1—Dc restored bubble (denoted by "1") and no-bubble (denoted by "0") differential sensor responses for a memory chip ensemble.

We describe a differential detection approach, and a circuit realization of it, which are insensitive to some signal amplitude, phase and shape variations in the DI, if these variations occur slowly when compared with the memory drive field period. The detector is based on the hypothesis that some signal function, such as peak-to-peak transition or the signal energy, is available in a DI such that the minimum functional change between unlike data pairs is greater than the maximum functional change between like data pairs in memory detection cycles that are contiguous. This condition must hold over the range of manufacturing and environmental changes in the sensor outputs for the chip ensemble, including noise and intersymbol interference effects. This proposed detector can be developed as a small inexpensive IC. It is easily incorporated in MBM circuit designs, and it is compatible with memory system requirements.

II. DIFFERENTIAL MBM SIGNAL DETECTION

2.1 Signal and interference characteristica of memory output

As indicated by the qualitative results shown in Fig. 1, the dynamic range of bubble and no-bubble responses in the DI may be significant across the desired operating range for an ensemble of a MBM chip type. However, for a given MBM chip and stationary operating environment, the responses for two data 1's (bubbles) or for two data 0's in successive DI's differ only through random noise and intersymbol interference (ISI) effects.

Sensor responses for bubble and no-bubble traversals depend on the memory sensor design, the chip technology, memory manufacturing quality control, and operating environment. Typically, the bubble response transitions of the MBM sensor in the DI have been in the 2-mV to 20-mV range, with a more restricted dynamic range over the ensemble and operating range of any particular memory type. Although unit-to-unit variations may exist in both bubble and no-bubble responses, as indicated by Fig. 1, a typical memory product gives a minimum transition difference of about 2 mV between the two responses in the DI.

When the phase of the DI is properly selected relative to sporadic random interference, such as magnetoresistive switching noise from the sensor or control signal cross talk, residual noise within the DI becomes a second-order effect. For example, the important frequency band of bubble signals in the DI is below 10 f_f, where f_f is the MBM field drive frequency. For MBM drive frequencies of less than 200 kHz, the signal processing band for a detector is then less than 2 MHz. For a 2-MHz noise equivalent bandwidth in a detector preamplifier, the total random noise within the DI is less than 50 μV rms referred to the output contacts of the MBM chip sensor. This includes random noise

from the MBM sensors under active memory conditions, the sensor bias current sources, and the detector electronics.

Fringe field coupling of bubble domains can exist across elements in a sensor array. This effect is observed as ISI in the DI response. Like the desired DI response, the ISI depends on the sensor array design and the memory operating conditions, but it is not well understood. Because of tbe nonlinear magnetic interaction of permalloy sensor arrays and bubble domains, accurate modeling and analysis of ISI as well as the desired bubble response have been intractable. In memory design, arrays have been selected to reduce tbe ISI, as well as random noise, to acceptable levels relative to the minimum difference between isolated bubble and no-bubble transitions in the DI. This condition is indicated by Fig. 2a for contiguous DIs for two signal amplitude cases. If ISI is severe for a memory design, this design can be changed or signal equalization can be considered for the detector.[4,5] However, because of the variable nature of ISI as well as tbe desired signal's shape in the DI, an equalizer should be adaptive. For typical useful DI durations of a few μs and very short setup times of the memory system, adaptive equalization of ISI is not cost effective in a bubble memory detector. By careful sensor design and processing control for the memory, it has been practical to hold ISI and noise to levels that permit differential detection with probability of error $P_E < 10^{-8}$ without using ISI equalization.

2.2 Data precoding and differential recovery from tha MBM

Figure 1 indicates that variations in the absolute levels, phases, and shapes of bubble and no-bubble responses along with a close match of like symbol responses in contiguous DIs make differential amplitude detection attractive for field-accessed MBM. This is analogous to differential phase detection used in communication cbannels.[6] If the binary data "1" is stored in the MBM chip as a bubble-to-no-bubble transition, or the reverse transition in contiguous memory cycles, then recovering data from memory is possible when the absolute values of the greatest DI response differences for pairs of like symbols are less than the smallest absolute values of differences for unlike symbol transitions. Figure 2b summarizes tbese prerequisite conditions for successful difference detection.

Direct difference encoding of tbe original data has the potential for propagating errors since a single error in decision can result in the loss of phase reference and cause ambiguity in the detector. This problem is eliminated by a simple precoding step for the data prior to recording. The precoding does not reduce the data throughput or storage capacity of the memory.

An original data sequence defined by $\{a_k\}$, where $a_k \in \{0, 1\}$ for k

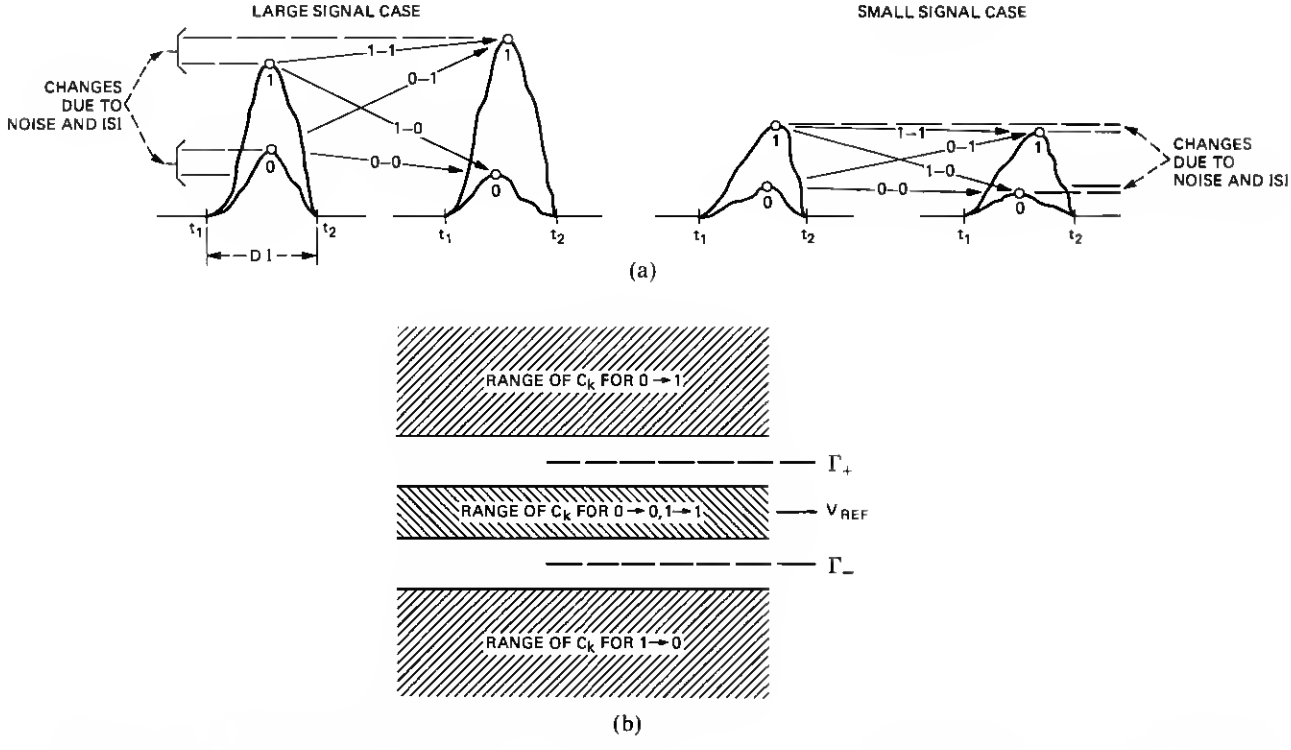

Fig. 2—(a) Dc restored bubble sensor response examples showing effects of dynamic range, ISI, and noise. (b) Response peak difference C_k ranges and Γ_+, Γ_- threshold placement.

≥ 0, is to be recorded as transitions between bubble and no-bubble states in consecutive field cycles in a way that eliminates propagating detection errors through loss of reference. This is accomplished by precoding $\{a_k\}$ into an equivalent sequence $\{b_k\}$, where $b_k \in \{0, 1\}$ for $k \geq 0$, by the algorithm

$$b_k = a_k \oplus b_{k-1}, \qquad \text{where} \quad b_{-1} = 0, \tag{1}$$

and $\oplus$ denotes modulo 2 addition. Then $\{b_k\}$ is recorded in the memory with a bubble state for $b_k = 1$ and a no-bubble state for $b_k = 0$. The precoding in (1) is implemented with a shift register and an EX-OR logic stage in the memory recording circuit.

If, in response to b_k, a functional B_k is available from the response in the DI and a decision of bubble or no-bubble in cycle k is to be based on B_k, difference detection is performed as follows. In the kth data cycle the analog difference $C_k \triangleq B_k - B_{k-1}$ is formed. Ideally, there are three possible analog levels for C_k corresponding to the four permutations of (B_{k-1}, B_k), and a ternary decision on C_k results in a three-state logic output $c_k \in \{-1, 0, +1\}$. In terms of the binary sequence $\{b_k\}$,

$$c_k = b_k - b_{k-1}, \qquad k \geq 0. \tag{2}$$

From expression (1), the modulo 2 subtraction of b_{k-1} from both sides of (2) gives

$$(c_k)_{\text{mod } 2} = (b_k - b_{k-1})_{\text{mod } 2} = a_k. \tag{3}$$

It follows then that $\{a_k\}$ is available by simple logic operations on the ternary sequence $\{c_k\}$ obtained from $\{C_k\}$ without the problem of error propagation due to phase ambiguity if a detection error occurs.

In practice, the differential detector outputs are estimates of the components of $\{c_k\}$ that are based on the available analog differences $\{C_k\}$. Then the detector outputs form the estimate sequence $\{\hat{c}_k\}$ and the estimate of the original data sequence is

$$\{\hat{a}_k\} = \{(\hat{c}_k)_{\text{mod } 2}\}, \qquad k \geq 0. \tag{4}$$

If in the kth cycle there is no detection error, $\hat{c}_k = c_k$ and hence $\hat{a}_k = a_k$. Figure 3 gives an example of the operations discussed in this section, where the functionals $\{B_k\}$ are the positive peaks of dc restored bubble and no-bubble responses in the detection intervals.

2.3 Choice of functional B_k

As discussed above, many variations can occur in the sensor responses from a given type of MBM chip which effect the shape, amplitude, noise content, and position of the responses in a DI. To successfully detect differences, any signal processing of the responses

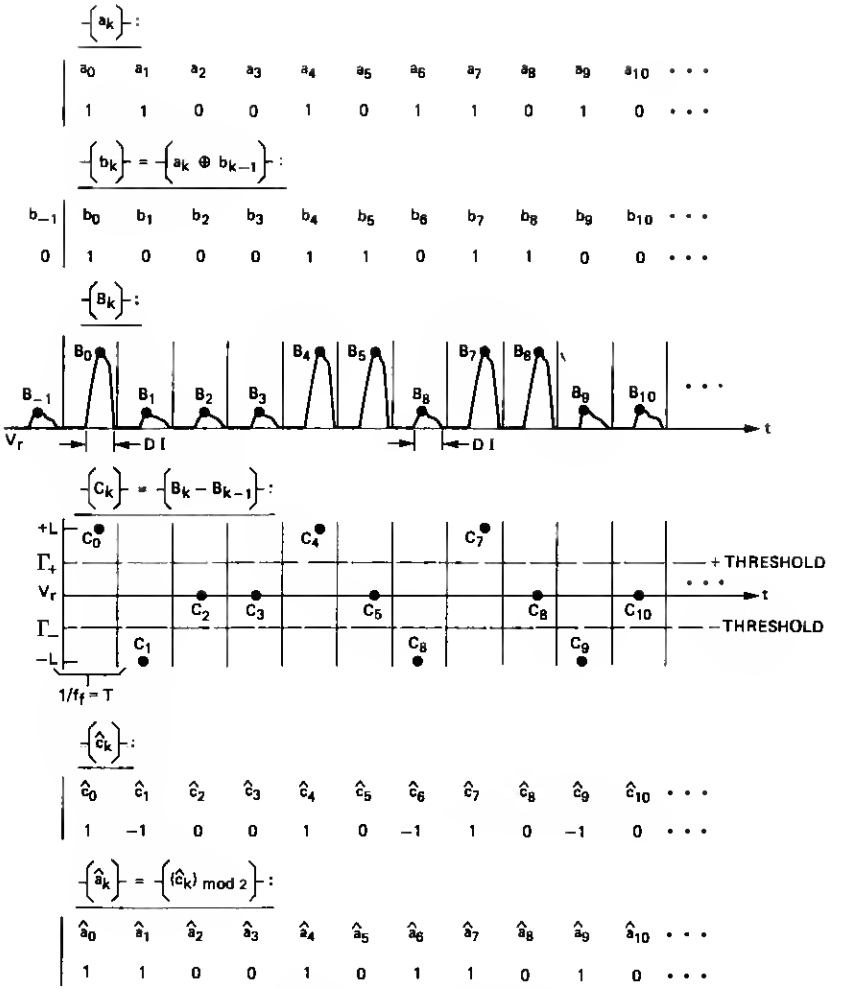

Fig. 3—Differential detection example.

leading to a sequence $\{B_k\}$ must result in nonoverlapping amplitude bands for the difference functionals $\{C_k\}$, as shown in Fig. 2b, in spite of the inherent variations in bubble sensor response. A diverse selection of practical approaches in signal processing can be considered to obtain $\{B_k\}$ from DI responses. Examples of processing over the DI for B_k are peak-to-peak acquisition, squaring-with-integration after dc restore, matched filtering of the nominal bubble response, and peak acquisition after dc restore. Each approach has advantages and disadvantages in detection error performance and detector circuit complexity for field accessed MBM signals as understood to date. Because of the difficulty

in modeling the statistical characteristics of the MBM signal and interference components, the analytical solution for a useful optimum detector has been intractable. The selection of any detector, and, in particular any signal processing approach to obtain $\{B_k\}$ for the differential detector considered here, has been based primarily on the performance observed in experiments with a representative ensemble of devices for each MBM design. The optimum choice of a detector is complicated additionally by practical considerations of its circuit realization, cost, and flexibility of operation.

Section 3 describes a differential detector tbat has been successful with signal characteristics of present bubble memories. This realization uses peak detection of dc restored signals in the DI to form $\{B_k\}$. We have found that signal equalization to reduce ISI and special noise filtering are not necessary in this detector for the bubble memory families of interest.

2.4 Detection errors and monitoring

In Section 2.2 the detected data sequence is

$$\{\hat{a}_k\} = \{(\hat{c}_k)_{\text{mod } 2}\}, \tag{5}$$

where $\hat{c}_k$ is the ternary logic sequence obtained by a bipolar threshold comparison of $C_k = B_k - B_{k-1}$. With the exception of noise and intersymbol effects in the generation of $\{B_k\}$, only two values occur for B_k under the conditions of static operation between memory detection cycles. Then of the nine combinations of c_k, c_{k+1}, the pairs (1, 1) and (−1, −1) can occur only through detection error. The sequence $\{\hat{c}_k\}$ can be monitored for the disallowed patterns as a simple error check, but this is not a complete error test.[7,8] Detection errors that yield valid c_k, c_{k+1} pairs cannot be detected by this simple monitoring. In general, an error within the memory that results in a recovered bubble sequence other than the $\{b_n\}$ that was recorded cannot be detected with this pattern monitoring. The altered bubble sequence in the MBM appears at the detector as a different $\{b_n\}$ sequence but one that could be generated by an admissible $\{a_n\}$ memory sequence.

Since the difference detector considered here involves the threshold comparison of $C_k = B_k - B_{k-1}$, it would seem that a detection error in recovery of $a_k = (c_k)_{\text{mod } 2}$ caused by a disturbance in acquiring a B_k would be highly correlated with a detection error in $a_{k+1} = (c_{k+1})_{\text{mod } 2}$ since $C_{k+1} = B_{k+1} - B_k$. This apparent coupling exists regardless of the data formatting discussed in Section 2.2 that is used for preventing error strings caused by detector reference loss. Whether it is more probable in difference detection to have an error pair given that one error occurs will depend on the method of generating functional B_k

and the interference that causes detection errors. It is known that in the case of additive Gaussian noise and matched filtering of signals without intersymbol interference, differential detection does not enhance the probability of double errors given single errors.[9]

III. A PARTICULAR DETECTOR CIRCUIT REALIZATION

The circuit shown in Fig. 4 performs the functions discussed in Section 2.2, including forming the functional $C_k = B_k - B_{k-1}$ required in difference detection. The system characteristics outlined below are compatible with available monolithic bipolar IC technology. Speed requirements implied by memory field frequencies up to 200 kHz seem to make bipolar technology essential at present for any analog difference detector type of IC. The realization of the functional C_k is simple; it requires a capacitor, a clamping switch, and a buffer amplifier. Then to obtain C_k it is not necessary to construct a true sample-and-hold for B_{k-1}, which is an advantage in bipolar circuit integration. All capacitors can be integrated and the complete bubble detector implemented as a single inexpensive IC with three synchronous input logic controls.

Figure 5 shows the key voltage waveforms for the circuit for the example data sequence $\{a_k\}$ in Fig. 3. To simplify the operating description, any voltage offsets in switches $SW1$, $SW2$, and $SW3$ are neglected as are the droop effects due to leakage currents from capacitors C_2, C_3, and C_4 when these are in their hold states. Adverse effects of switch offsets in an IC realization of the circuit can be eliminated by component trims during manufacture. At points in the circuit where leakage currents from capacitors are critical to performance, bipolar field effect transistor (BIFET) amplifier isolation is assumed; these are shown in Fig. 4. BIFET amplifiers have bias requirements on the order of 1 nA within a circuit ambient range of [−10°C, + 70°C].

The data cycle period in Fig. 5 is $T = 1/f_f$, where f_f is the MBM drive field frequency. The signal detection interval (DI) is $[t_1, t_2]$, modulo T. The other intervals of interest are $[t_3, t_4]$, modulo T, where switch $SW2$ is closed, and $[t_5, t_6]$, modulo T, where C_3 is discharged through $SW3$. The maximum operating field frequency is limited by the bubble memory technology. The period T considered for the differential detector design is in the range [5 μs, 40 μs].

In each DI, the B_k acquired is the maximum of the peak catcher input

$$e_1^* = e_1 - e_{c2}(t_1) + V_r, \qquad \text{for} \quad t \in [t_1, t_2], \text{ modulo } T, \tag{6}$$

where $e_{c2}(t_1)$ is the initial condition of the voltage across C_2 at the start of the DI, and V_r is the switch voltage reference. The value of $e_{c2}(t_1)$ is a function of $e_1(t)$, for $t \leq t_1$, as well as the filter action provided by the R_{02}, C_2, R_{s1} circuit when $SW1$ is closed. The noise that

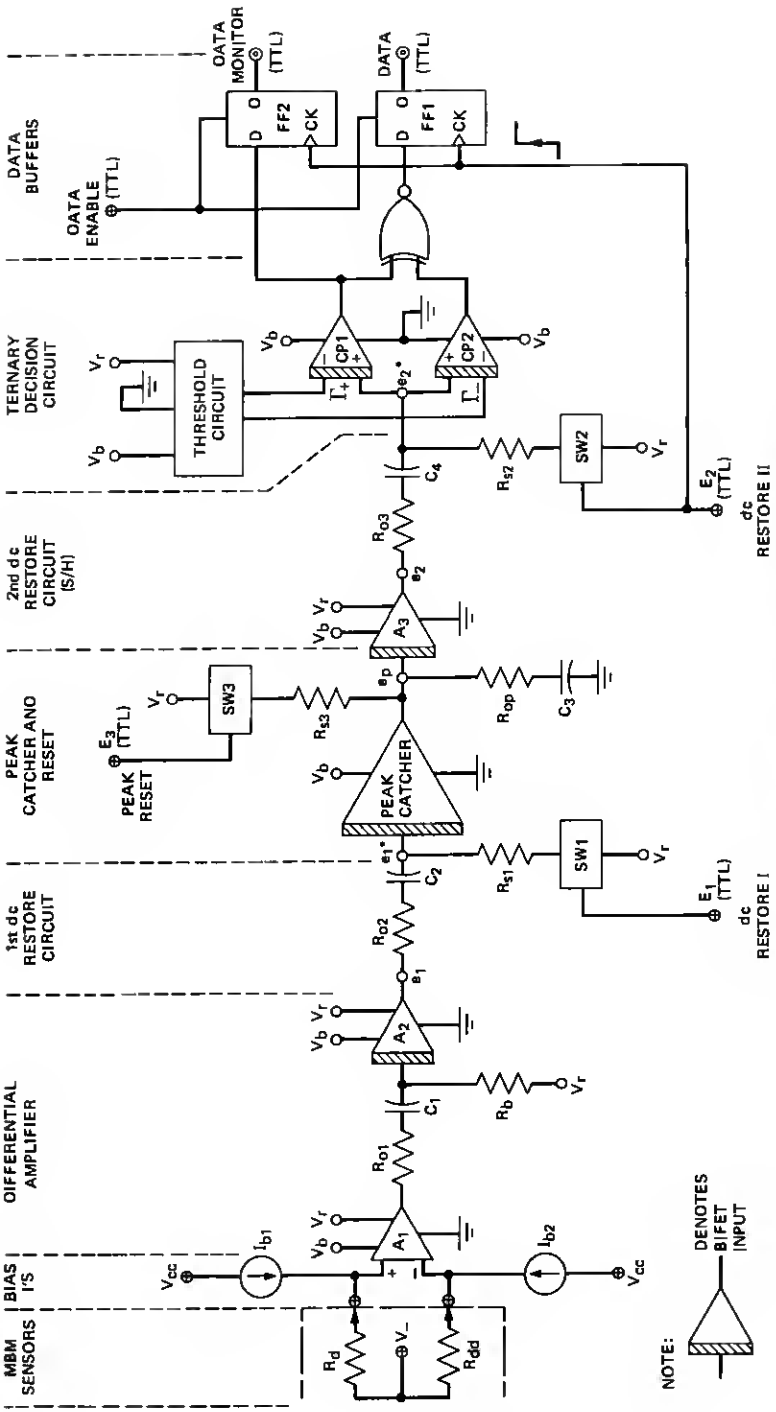

Fig. 4—Differential detector for magnetic bubble memory sensor outputs.

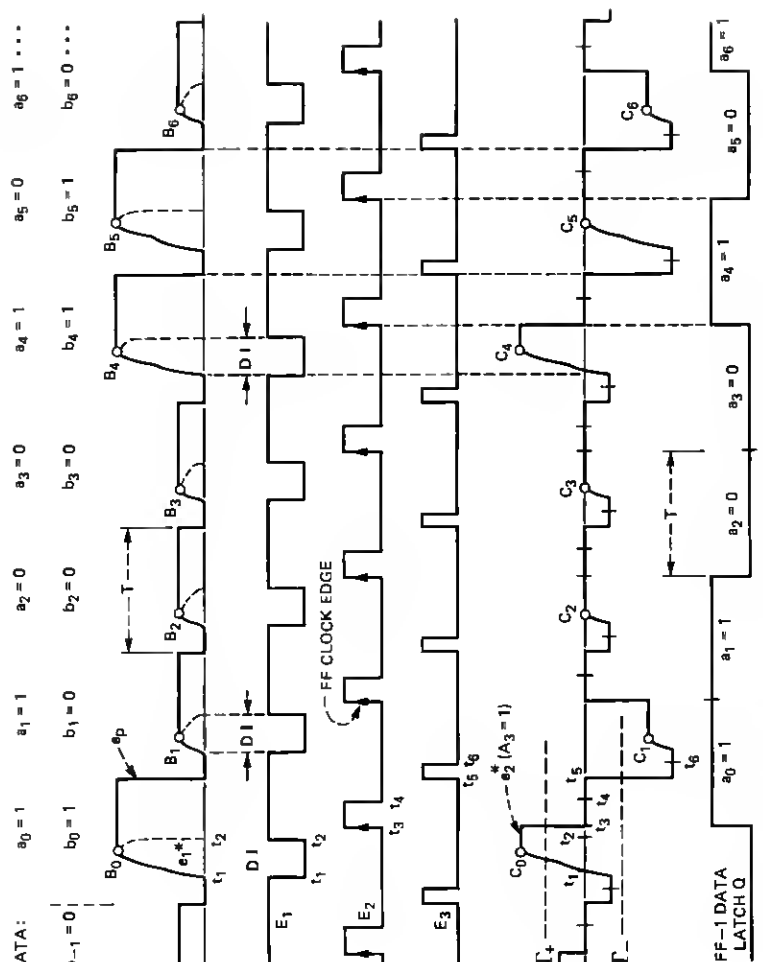

Fig. 5—Ideal signal and timing sequence example for differential detector.

is present with the desired signal input e_1 of the dc Restore I circuit is enhanced in the restored signal e_1^*. Because of this, a nonzero time constant, $\tau_a = (R_{02} + R_{s1})C_2$, can be advantageous. If $\tau_a \to 0$, then $e_{c2}(t_1) \to e_1(t_1)$, and $e_1^*(t_1) \to V_r$, which gives an exact restoration of e_1^* to reference V_r at t_1. But then the steady state noise variance of e_1^* in DI is twice the noise variance of e_1.

The functional B_k is retained on the storage capacitor C_3 until discharged by a HI state of E_3 during $[t_5, t_6]$. With E_2 held LOW during the DI as well as the PEAK RESET interval, the Restore Switcb II output e_2^* follows the acquisition of B_k and the reset transition that occurs in the peak catcher output e_p when C_3 is reset by $SW3$. When E_2 is HI, $SW2$ is closed, and a voltage e_{c4} is stored across C_4 that is a function of both $e_2(t)$ for $t \in [t_3, t_4]$ and the filter time constant $\tau_b = (R_{03} + R_{s2})C_4$. Then for $t \in [t_4, T + t_3]$, modulo T, $SW2$ is opened, and the comparator (+) input is

$$e_2^* = e_2 - e_{c4}(t_4) + V_r. \tag{7}$$

If $\tau_b \to 0$, then $e_{c4}(t_4) \to e_2(t_4)$ and an exact restoration of e_2^* to V_r occurs. But if noise is present in e_2, the filtering provided when $\tau_b \neq 0$ may result in improved performance to a degree that depends on the signal and noise characteristics of e_2.

For the time sequence of controls, E_1, E_2, and E_3 shown in Fig. 5, the value of $e_2^*(t)$ when $t = (kT + t_3^-)$ and $k = 0, 1, 2, \cdots$, is $A_3C_k = A_3(B_k - B_{k-1})$, where A_3 is the gain of the second interstage amplifier. When, in response to like and unlike symbols in the data pair (b_{k-1}, b_k), the analog values $C_k = B_k - B_{k-1}$ lie in three nonoverlapping bands, as shown in Fig. 2b, the recovery of the original sequence $\{a_k\}$ follows from the trilevel comparison of each A_3C_k value with a threshold pair (Γ_-, Γ_+). If $A_3C_k \geq \Gamma_+ = V_r + \gamma_+$, the trilevel logic response is $c_k = +1$; if $A_3C_k \leq \Gamma_- = V_r - \gamma_-$, the decision is $c_k = -1$; and for all other values of A_3C_k, $c_k = 0$. Then from eq. (3), the original sequence $\{a_k\}$ is the output of the EX-NOR gate in Fig. 4. Amplifier A_3 in conjunction with the dc Restore II circuit provides the desired differencing C_k in each detection cycle. A complete sample-and-hold function is unnecessary since the difference C_k and not the absolute levels of B_k and B_{k-1} are required for differential detection.

In the kth data cycle, a_k is latcbed in $FF1$ by E_2. The same positive edge of E_2 clocks $FF2$ to latcb the logic level out of comparator $CP1$. The DATA and DATA MONITOR outputs are sufficient to detect invalid (c_k, c_{k+1}) pairs $(+1, +1)$ and $(-1, -1)$ that may occur if there are detection errors. This was described in Section 2.4.

IV. DETECTOR OPERATION EXAMPLE

The detector shown in Fig. 4 was constructed from discrete BIFET and bipolar transistor devices that are typical of those that could be

used in making a monolithic linear IC. Table I lists a summary of the conditions for this discrete component circuit. We chose the parameters listed in Table I, including values of the two thresholds Γ_+ and Γ_-, for an MBM type that seems to be typical of the field-accessed bubble-memory art. For other MBM device designs, it may be desirable to have different parameter values than those considered here to maximize detection performance.

Fig. 6a shows superimposed bubble and no-bubble responses for e_1 and the restored signals e_1^* and e_2^* for a recorded $\{b_n\}$ sequence in the MBM that is the periodic hexadecimal pattern ABEF5410. One of the two orthogonal coil currents, I_x, that comprise the bubble memory square wave drive field, is shown also. In the e_2^* trace of Fig. 6a, the detector "EYE" diagram is formed by the three levels at the right side of the peaks of e_1^*. The levels of this EYE correspond to the trilevel logic outputs $c_k \in \{-1, 0, +1\}$. The thresholds Γ_+ and Γ_-, at the negative inputs of comparators *CP*1 and *CP*2, are positioned within the EYE to get minimum detection error probability over the memory ensemble and its range of operating conditions. Nonadaptive detection is possible if Γ_+ and Γ_- can be placed between the center band and the upper and lower bands of the e_2^* EYE. The difference detector performance is immune to the absolute levels of the peaks of e_1^* that occur within the detection intervals, but it does depend on the minimum change in peaks for unlike contiguous data pairs and the maximum change for like data pairs. The widths of the EYE are determined by

Table I—Detector Parameters

1. Sensor resistances: R_D, $R_{DD} = 1600\ \Omega$
2. Bias currents: I_{B1}, $I_{B2} = 3.75$ mA
3. *SW*1 filter time constant: $[R_{02} + R_{s1}]C_2 \cong 60$ ns
4. *SW*2 filter time constant: $[R_{03} + R_{s2}]C_4 \cong 60$ ns
5. Amplifier A_1: gain = 10, 3 dB frequency = 3 MHz, critically-damped two-pole response.
6. Amplifier A_2: gain = 5, 3 dB frequency = 3 MHz, two-pole response with 1 dB overshoot.
7. Amplifier A_3: gain = 3, frequency response same as A_2.
8. Capacitors: C_1, C_2, C_3, $C_4 \cong 50$ pF.
9. Resistors:
   R_{01}, $R_{0p} \cong 200\ \Omega$,
   R_{02}, $R_{03} \cong 10^3\ \Omega$,
   R_{s1}, R_{s2}, $R_{s3} \cong 200\ \Omega$,
   $R_b \cong 10^6\ \Omega$.
10. Thresholds*:
    $\Gamma_+ = V_r + \gamma_+ +$ [closed *SW*2 offset],
    $\Gamma_- = V_r - \gamma_- +$ [closed *SW*2 offset],
    γ_+, $\gamma_- = 345$ mV.
11. Voltages: $V_b = 10V$, $V_r = 4V$, $V_{cc} = 12V$
12. Leakage currents: For e_1^*, e_p, and e_2^* nodes, current leakages are approximately 1 nA.

* The thresholds Γ_+ and Γ_- are offsets from the reference voltage {V_r + [Closed *SW*2 Offset]} of the comparator input e_2^*. This is shown in Figs. 4, 5, and 6. The optimum values for the offsets, γ_+ and γ_-, are determined by the particular properties of the bubble memory family for which differential detection is considered. For the memory code under investigation here, the values selected were $\gamma_+ = \gamma_- = 345$ mV.

the difference between bubble and no-bubble signal transitions in the DI and by intersymbol interference and noise. The effect of noise has been of secondary importance when DI is properly selected. Also, through proper MBM sensor design, ISI effects due to bubble coupling in the sensor array can be held to an acceptable fraction of the minimum isolated bubble and no-bubble difference. The signal, noise, and ISI are all functions of the MBM design.

Figure 6b shows the timing sequence of E_1, E_2, and E_3 relative to the response e_2^* out of the Restore Switch II for the sequence $\{b_n\}$ at an isolated 1 subpattern $\cdots, 0, 0, 1, 0, 0, \cdots$. This e_2^* waveform contains small voltage steps that coincide with the logic level shifts in E_1, E_2, and E_3. These steps are not sbown in the idealized e_2^* response in Fig. 5, but they can occur in a real circuit that has nonzero switch offset voltage or stray capacitance feedthrough of switch control logic into the signal path. Because the detector bases decisions on tbe difference $C_k = B_k - B_{k-1}$ each cycle, the effects of switch offsets and feedthroughs can be eliminated by equating the contributions from $SW1$ and $SW3$ while trimming thresbolds Γ_+ and Γ_- during IC manufacture to account for $SW2$ offset.

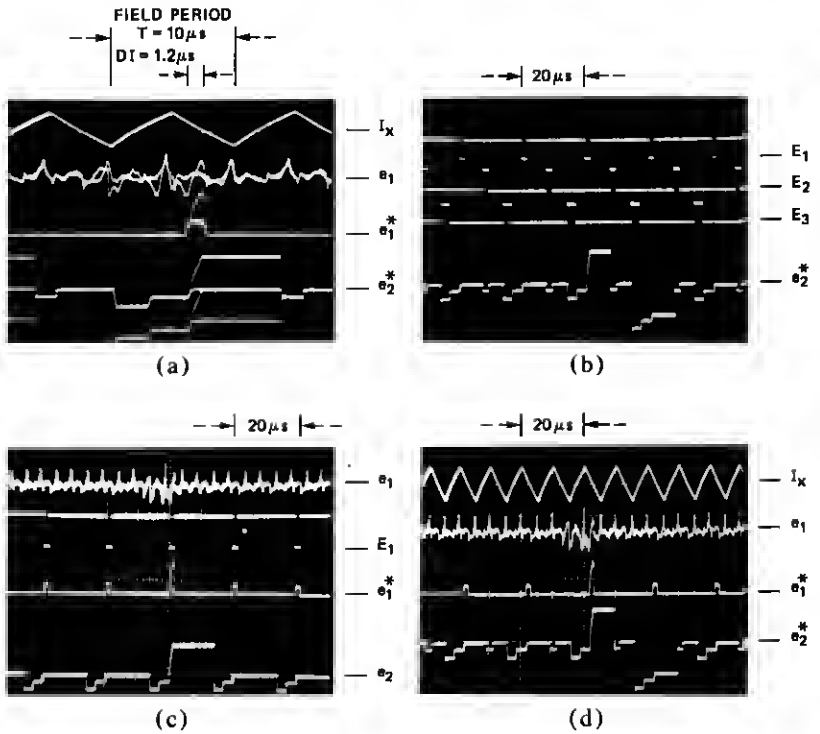

Fig. 6—Signal and control waveforms for differential detector.

Figure 6c shows the peak catcher response e_2 after amplification by A_3 for the $\{b_n\}$ subpattern $\cdots, 0, 0, 1, 0, 0, \cdots$. The trilevel response e_2^* in Fig. 6b corresponds to this e_2 pattern, and is obtained by clamping e_2 at $SW2$ when E_2 is HI.

Figure 6d gives another comparison of the detector signals for the $\{b_n\}$ sequence $\cdots, 0, 0, 1, 0, 0, \cdots$. The test patterns in Fig. 6 were obtained for a bubble memory device where no-bubble cycles were interleaved with the data cycles. The interleaved no-bubble responses are present in the e_1 waveforms but have been suppressed in e_1^*, e_2, and e_2^*.

V. CONCLUSIONS

We have described a magnetic bubble memory detector that will make correct decisions from memory sensor outputs even when large environmental or chip-to-chip signal transition variations occur in the detection interval (DI). The only constraints for successful detection are that for the selected functional B_k the maximum differences in $C_k = B_k - B_{k-1}$ for like symbols in contiguous data cycles are less than the minimum differences for unlike symbols. When the DI is properly selected to minimize interference, these constraints appear to be acceptable for typical outputs from a MBM design when the environmental changes in memory operation are slow relative to the field drive period.

At memory start up, the detector must have at least one cycle of output from the chip sensors in order to initialize. When input data $\{a_n\}$ is encoded to eliminate error propagation, then the recorded sequence is $\{b_n\}$, where $b_{-1} = 0$, and a single no-bubble sensor response is needed to initialize the detector. The comparison of sensor output to the uninitialized discharged reference condition in the detector circuit in the first read cycle can produce a single error if the first data bit in the $\{b_n\}$ data block is no-bubble. This is possible since a memory chip may have a no-bubble response B_k in excess of the optimum differential thresholds Γ_+ and Γ_- set in the difference detector. This detector-initializing no-bubble cycle is not a significant memory system constraint.

The detector circuit considered here incorporates peak sensing in a detection interval of the dc restored sensor response to generate the B_k each data cycle. Other forms of signal processing can be used to obtain B_k. In particular, if input noise is a problem in future MBM designs, the sensor outputs could be dc restored and integrated or matched filtered without dc restoration over the detection interval. But the resulting "1" and "0" responses for B_k must be sufficiently different to guarantee a detectable EYE. Also, if memory device design results in excessive intersymbol interference (ISI), signal equalization

can be considered to improve detection. At present, peak detection of bubble transitions with threshold comparison of $C_k = B_k - B_{k-1}$ seems to be adequate for differential detection of field-accessed MBM outputs. ISI equalization and special care in noise filtering have not been required to obtain a consistent differential detection probability of error below 10^{-8} for the memory types considered.

In light of the disadvantages frequently encountered with adaptive detectors and the advantages of a bubble memory detector that can accommodate a wide dynamic range for chip sensor response transitions, the differential detector described here has considerable merit. It is reasonable to integrate this detector as a monolithic bipolar IC such that the bubble memory detection step is accomplished by a single self-contained inexpensive DIP. Size and cost as well as the detector performance are very important memory system considerations, since even a modest bubble memory system can require many independent detector circuits.

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